FMS-DE Discrete Electrical Networks

Enabling advanced Real Valued Modelling for complex modules and SoCs by providing analog wire functionality for Verilog simulators.

Presilic

FMS-DE provides a low cost ready-made feature rich alternative to in-house UDN implementations of discrete analog wires in SystemVerilog, needed as part of SoC pre-silicon mixed signal functional verification. With basic features such as resistive and ideal networks, multiple channels, and current and voltage resolution, as well as additional features such as limits checking, wire state checking, signature values, wire debug, and AMS connect modules, FMS-DE promotes ease of use and high productivity.

Introduction

Real Valued Modelling (RVM) refers to functional analog models which compute electrical quantities using real valued expressions in discrete time. Typically these models are written at module -level and used for System-on-Chip (SoC) pre-silicon functional verification. RVM is highly effective in the detection of SoC-level connectivity errors and inter-module behavioral dependencies not encountered during module-level characterisation and verification.

RVM is employed when Spice/AMS excessive simulation times preclude either mixed signal verification at SoC level or exhaustive testing of highly configurable designs at module-level.

For anything but trivial systems, RVM requires analog connectivity, usually with both voltage and current resolution, and in some domains multiple channels per connection. SystemVerilog 2012 introduced a new language feature, User Defined Nets, which enables custom implementations of analog wires. FMS-DE provides an alternative easy to use, cost effective, ready-made solution.

Discrete Electrical Networks

FMS-DE provides Discrete Electrical (DE) networks, which comprise analog wires supporting voltage resolution and conservation of current consistent with Kirchhoff's voltage and current laws. DE network drivers and sinks may be dynamically configured as resistive or ideal. FMS-DE networks also support multiple channels (multiple independent networks sharing the same connectivity), and ideal switches which are essential for the implementation of muxes. A network/channel state and associated warning messages provide information on, for example, whether a network is undriven, or whether two or more (parallel) ideal voltage sources are simultaneously enabled. Debug features provide yet further information.

When using the default FMS-DE implementation, network connectivity is established using VPI, and DE networks are superimposed on the 4-state structural connectivity formed using standard Verilog wire module ports and connections, and therefore requires no changes to port or wire types when netlisting hierarchy. Furthermore, 4-state values may still be driven onto the underlying 4-state connectivity.

Functional API

DE networks are driven/monitored using source/sink components provided in the form of SystemVerilog modules. Voltage and current are set and monitored using instance variables. A network state variable is also available for checking whether the network is being driven correctly. A separate set of variables for control and monitoring is provided for each (independent) channel.

Additional tasks / functions / variables are provided for setting and checking of limits on monitored variables, and for providing additional debug information, such as which sources/sinks comprise the network and their current state.

FMS-DE provides a standard set of both single and multi-channel components, including a multi-channel ideal switch. If needed, Presilic may provide components with a non-standard API specific to customer requirements, where this is practical/feasible. Customers can also create their own components if they wish, based on the functionality available.

Signature Values

In addition to issuing warnings and setting status variables when a channel's configuration is invalid (eg two ideal voltage sources in parallel enabled simultaneously), FMS-DE overrides that channel's monitored value with an instantly recognisable constant value (eg 2.02020202e-12) to provide a visual indication of the network / channel's state. This provides a visual cue when viewing waveforms.

Co-simulation with Spice/Verilog-AMS

Single channel connect modules and connect rules are provided for integration with Verilog-AMS. These connect-modules dynamically support ideal and resistive networks, and their A2D sensitivity can be set by DE network components, in order to optimise the number of conversions, especially in cases where analog noise is present.

SystemVerilog UDN Option

An optional FMS-DE implementation is also available where network connectivity is established using SystemVerilog User Defined Nets, rather than VPI. A comparison of the implementations is shown in Figure 1.

Feature / Limitation	VPI	SV UDNs
Analog elaboration with HUGE designs	potentially slower	potentially faster
Channel potential viewable on net segments in waveform viewer	✗	✓
Connectivity through protected envelopes	✗	✓
Simulator additional license feature	✗	✓
Coexistence with 4-state	✓	✗
Multiple network types / UDNs on the same net	✓	✗
Need to parameterise multi-channel switch based on type	✗	✓
Co-simulation with AMS	✓	✓

Figure 1: comparison of VPI and SV UDN connectivity implementations

Key Features

- resistive and ideal networks
- voltage and current resolution
- single and multi-channel
- ideal multi-channel switch
- coexistence with 4-state
- connect modules for AMS/Spice co-simulation
- network state monitoring, and network debug
- signature values
- transient condition warning controls
- SystemVerilog UDN connectivity option
- project / file based configuration of features
- ready-made
- extensible

Availability

FMS-DE is licensed software, provided as SystemVerilog modules and VPI libraries, available on Linux for the following simulators:

- Cadence® Xcelium
- Mentor® Modelsim / Questasim

Contact us regarding use with other simulators. FMS-DE will soon be available for use on Windows® platforms.

Support

Presilic provides email support as standard, as well as dedicated maintenance contracts where required.